Modeling for the Balance Network for Common Mode Noise Suppression

Parasitic capacitance is extremely important to the issue of electromagnetic interference (EMI) because most of common mode (CM) noise is conducted through parasitic capacitance. For balance technique, the self-resonance between the coupled inductor and its parasitic capacitance also deeply affects the impedance of the balance network. In this paper, the reason of the ineffective CM noise reduction beyond 10 MHz with balance technique is investigated. Taking the inter-turn and inter-layer capacitance of the PCB-based coupled inductor into consideration, the balance network model is based on the experimental result. The root reason of the failure of high coupling coefficient is articulated. According to the analysis, an improved inductor structure is proposed and the effectiveness of the new structure is validated.

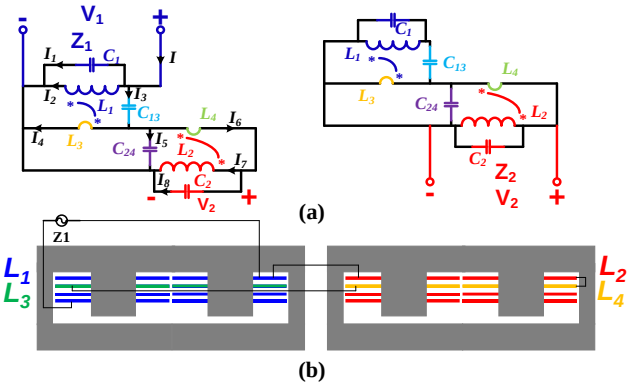

Fig.1. (a) Reorganized balance network circuit (b) Coupled inductor physical connection

Fig. 1 (a) is the reorganized balance network with the inter-layer and inter-turn capacitance. The left one is a Z1 measurement equivalent transformer circuit and the right one represents Z2. Fig. 1 (b) is the physical connection. C1 is the inter-turn capacitance of L1, while C13 is the inter-layer capacitance between L1 and L3.

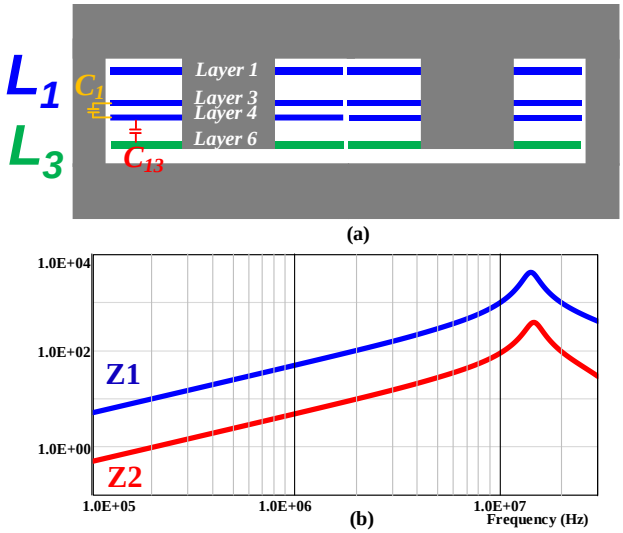

Fig. 2. (a) Improved coupled inductor structure (b) Measured impedance

It is important to decrease the interwinding capacitance. L3 is in the middle of L1, which is used to reduce the winding loss. But this configuration also doubles the inter-layer capacitance since both the top layer and bottom layer are L1. Fig. 2 (a) is the improved version of the coupled inductor. L3 is moved to the bottom of L1. Meanwhile, the layer distance between L3 and L1 is increased to ensure the lower inter-layer capacitance. Since there are 6 layers in the PCB, layers 1, 3, and 4 are used for L1 and layer 6 is used for L3. The impedance of the improved coupled inductor is shown by Fig. 2 (b).